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SiC at its Best...! or Customer Specific SiC Modules

While the speed of development for power electronics is increasing and possibilities of technology are exponentiating, today developers have various choice of which device to choose. The following article intends to get an overview for the various technologies and innovations in packaging technologies for customer specific SiC power modules.

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The field of power electronics is aiming at three important goals: miniaturization of devices while increasing the power density and reducing the losses. In the past there have been different approaches to achieve those goals

One approach is the use of different materials. Silicon replaced Germanium very quick and has been hold as "philosopher's stone" for a long time. With the wide band gap materials the revolution in the power electronic industry starts again.

Due to the wide band gap as well as very good thermal conductivity SiC and GaN are ideal for high break down voltages, high frequencies and high temperature operation. Due to the structure of cost (yield and \$/cm²) and the figure of merit for GaN-HEMTs (High Electron Mobility Transistor) the expected domain of GaN devices will be in application with break down voltages below 1200V, while the domain of SiC will be for break down voltages greater and equal to1200V. [1]

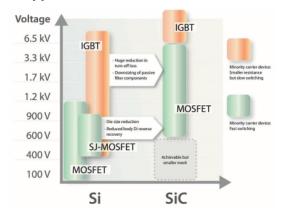


Figure 1: Overview of different power semiconductors in different voltage classes for Si and SiC SiC- und GaN-power devices

One further approach is the power device topology. Until the 1970s the bipolar Transistor has been state of the art. Due to its voltage dependent behavior, positive temperature coefficient and low conduction losses the MOSFET could replace the bipolar transistor.

With the introduction of the IGBT in the 80s advantages of the bipolar and FET structure could be combined. Nowadays both MOSFET and IGBT have their operating area dependent on the intended frequency

and blocking voltage. While the IGBT is generally used for low frequencies (<30kHz) and high blocking voltages (>1000V) the MOS-FET is used for higher frequencies (>=20kHz) and lower blocking voltages (<400V)

In the overlap segments where MOSFET and IGBT can be used it depends on the customer's application. Also special developed FETs like the SJFET are dominant in this market segment.

With introduction of SiC- and GaN-power devices the hunt for the best topology starts again. Today SiC-MOSFET, -JFET and -BJT are commercially available.

Due to the good adaption to Si devices a trend can be seen for the MOSFET. CREE and other mayor vendors are going for the normally-off MOSFET. Other companies go for the JFET (mostly normally-on) because of its higher current capacity. The problem with the normally-on structure with the GaN-HEMT or the SiC-JFET can be solved by a series connection of a Low-Voltage Si MOSFET (Cascode circuit). As another big player Fairchild is going with the BJT for the bipolar structure.

Although, the use of SiC-diodes and -transistors have made a big progress in some applications there are two more mayor problems to be solved before SiC can fully penetrate the market: pricing and package

Compared with Si-power devices on a discrete Level the price per device for SiC is multiples time higher.

At the discrete component level, the price per component part is higher compared to the Si power semiconductors due to the fact that the production is limited to 4" SiC wafers at the moment and SiC is a very expensive material. There will, however, be a significant improvement in terms of pricing in the medium term, because the surface of a SiC MOSFET is considerably smaller than an Si-IGBT and CREE e.g. can switch over to 6" wafers should the demand continue to increase.

Upon introduction of a 1700V, 10hm SiC MOSFET (C2M1000170D), CREE can even offer a MOSFET which, in terms of price, is able to keep up with the Si-MOSFETs with a reverse voltage of more than 1200V - and has a significantly better performance. Furthermore, CREE, apart from the second generation of the 1200V, 80mohm

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MOSFETs, has now also launched the second generation of the 1200V, 160mohm MOSFETs (C2M0160120D). In the second generation of SiC-MOSFETs, a considerably improved price could be achieved by a reduction of the chip area. Moreover, faster turn off and a better overall performance can be obtained by means of the expanded input voltage range (V_{GS}=-10V/+25V) and the lower capacitance. All MOSFETs are available ex stock MEV Elektronik Service GmbH.

A comparison of the price in relation to the overall system costs shows a considerable reduction of switching losses and a reduction of costs in certain applications. The advantages offered by the characteristics of the SiC technology such as the higher switching speeds or extremely low losses can e.g. lead to cost savings with regard to inductor or heat sink.

Integrated circuit packaging

Apart from the price, another significant item is the housing or more precisely the integrated circuit packaging. On the one hand, the market requires the adaptation of standard packages, in order to reduce time and effort and the costs of a design-in. On the other hand, the available packages are hardly appropriate for the requirements and possibilities of SiC and GaN due to insufficient heat dissipation.

With identical RDS,on, a SiC-MOSFET has a 33 times, respectively 10 times smaller chip area than a Si-MOSFET or Si-SJFET. A reduction of the chip surface also leads to a reduced gate charge Qg and overall capacitance C, which are substantial factors for the losses. Fig. 2 shows the development of the chip surfaces in the past years.



Figure 2: Development of chip area with respect to junction temperature in power electronics [2]

Due to the fact that the ratio between power loss and available module surface steadily increases, the type of cooling (air, liquid) is another important element apart from the thermal transfer. Various packaging technologies and chip carrier substrates are now also available here.

Powersem packages

Since 2013, MEV Elektronik Service GmbH has been cooperating with Powersem GmbH, a German manufacturer and innovator of customized SiC modules.



9 mm Bauhöhe

9 mm Bauhöhe



6 mm Bauhöhe







7 mm Bauhöhe 12 mm Bauhöhe Eco-Press-Fit® mit Bodenplatte

SOMESEM



5.5 mm Bauhöhe

he 12 mm Bauhöhe ohne Bodenplatte

Bauhöhe variabel Chip on Heatsink®

Figure 3: Selection of several Powersem packages with different overall heights. SiC-EcoTM 1 and SiC-EcoTM 2 9mm and 17mm overall height, SOT-227 12mm overall height, Subassembly variable overall height, SiC-SlimTM 6mm overall height, Eco-SMPDTM 5.5mm overall height, Eco-227TM 12mm overall height without base plate, Chip-on-HeatsinkTM (CoH) variable overall height

"With the Eco- 227^{TM} , we have responded to the customers' needs without losing sight of the significantly improved characteristics of the SiC chips" says Mr Chadda, Managing Director of Powersem GmbH. "Due to the same housing and mounting dimensions as with the SOT-227, the customer is provided with optimum adaptability without being forced to convert his production. Consideration is given to the chip by mounting the Eco- 227^{TM} without additional base plate." Further examples are the SiC-Eco 1, SiC-Eco 2 and SiC-Eco 3 with a module overall height of 6mm, 9mm or 17mm. The SiC-Eco TM family is available both as solder able and as press-fit versions (Eco-Press-Fit TM). The Eco-SMPD TM (see figure 3) is also completely new and, compared to conventional TO-247 or TO-264 packages, it excels in low parasitic capacitances, low thermal resistance and high electrical voltage isolation.

Furthermore, Powersem is able to use the "Chip-on-HeatsinkTM" technology in its module concepts. "Chip-on-Heatsink™" is an innovation by CeramTec GmbH. As a manufacturer of high-performance ceramics, CeramTec is an important supplier for the power electronics industry. In the Chip-on-Heatsink technique, a copper layer is applied and sintered onto a ceramic base plate. These techniques are well known e.g. from thick-film technology. Thus, the ceramic material replaces the former base plates made of copper or AISiC and provides the electrical isolation. The use of copper provides excellent electrical and thermal conductivity. The chip is directly soldered onto this copper layer. Due to this technique, a large number of thermal resistors can be omitted. Depending on the required ampacity and heat distribution, the copper layer may have a thickness of up to 400µm. Depending on the layout, the intimate bond between copper and ceramic material brings about a slightly convex bottom plate which is extremely beneficial for the heat-transmitting mounting on a heat sink.

Chip on Heatsink offers perfect preconditions for the reduction of the thermal resistance, in order to effectively distribute heat from the SiC chips. This feature as well as the thermal cycle-ability, which is about 10 times higher compared to the previous standard technologies, may lead to considerable improvements in power electronics.

The base plate cannot only be designed as a flat plate but also as a heat sink with integrated fins for convection cooling. Due to the fact that the base plate and the fins consist of one part, the normally necessary thermal heat sink paste or soldering can be omitted. If even higher losses are dissipated, the use of ceramic material enables the design of highly efficient liquid coolers. Here, the copper layer is directly applied, too, and represents the conductive paths, onto which the dies are directly soldered or sintered without any further interface.

Substrate chart

Nowadays, the three most commonly used substrates are AL2O3, AIN and Si3N4. Apart from the costs, the different physical properties such as thermal conductivity, thermal capacity, heat distribution and the coefficient of thermal expansion have to be taken into account. Table 1 shows an overview of the physical properties and a general cost overview for AL2O3, AIN and Si3N4.

expansion of the thick-film technology towards considerably higher currents and performances.

Summary

It has been stated that not only the appropriate package is vital for the selection of the right module but above all the right selection of substrates and technology. Usual distributors are dependent on the

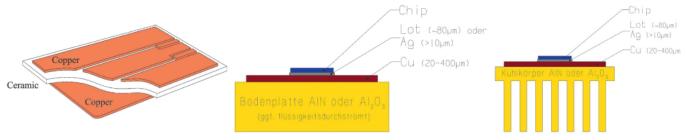


Figure 4: left-hand: DCB with double-sided copper [3], middle: cross section of SCT design with base plate or liquid cooler, right-hand: cross section of SCT design with liquid cooler

A high thermal conductivity value indicates a higher heat transmission per unit of time. The breakdown voltage specifies which maximum field strength an insulating material can withstand under certain conditions without losing its insulating properties. The coefficient of thermal expansion describes the relative change of length in case of a change of temperature.

	AL ₂ O ₃	AIN	Si ₃ N ₄
Thermal conductivity @20°C [W/mK]	24	180	90
Breakdown voltage [KV/mm]	10	20	18
Coefficint of thermal expansion @20°C - 300°C [ppm/K]	6.8	4.7	2.5
Costs Nov 2013	low	high	very high

Table 1: Physical properties and cost appraisal of different substrates [2]

While the cost appraisal in general clearly speaks in favor of AL_2O_3 , AIN and Si_3N_4 have obvious technical advantages compared to AL_2O_3 . The better thermal conductivity of AIN compared to Si_3N_4 may be put into perspective taking into consideration that with Si_3N_4 only substrate layers which are half as thick can be used. Another big advantage of Si_3N_4 is the higher thermal stability against alternating loads. The thermal stability against alternating loads depends to a great extent on the technology applied.

DCB, AMB and SCT

Direct copper bonded (DCB) or Direct Bond Copper (DBC) comprises the application of copper onto insulation (ceramic material) by means of a high-temperature process, which very firmly bonds the copper to the ceramic material. The copper layers normally have a thickness of 200 or $300\mu m$ which makes fine structures impossible.

Similar applies to AMB, where a copper film is firmly bonded to a ceramic plate by means of a high-temperature soldering process across the entire surface. Then the insulation trenches are etched in both processes.

With SCT, the process is different. Here, the copper layer is applied onto a ceramic plate up to a thickness of 400µm, namely only where it is desired. Due to the processes applied, almost any thicknesses can be produced. Furthermore, not only ranges with thin and very fine structures (100µm pitch) but also ranges with thick copper with a high ampacity are possible on a substrate. Thus, SCT represents an

existing technologies of their suppliers and have to sell their available product portfolio to the customers. As a design-in distributor, MEV, however, strongly focuses on technical competence. Accordingly, well-known manufacturers are working on customized projects together with MEV, thus guaranteeing that the customer is able to decisively contribute to the development of the desired module.

	AL ₂ O ₃	AIN	Si ₃ N ₄
	Medium (can be improved by Dimple)	'	Very good
	Medium (can be improved by Dimple)		Very good
SCT [cycles]	Very good	good	Very good

Table 2: Thermal stability against alternating loads with different substrates and technologies

CREE Inc., Powersem GmbH and CeramTec GmbH are strong and innovative partners of MEV Elektronik GmbH who perfectly match the customized design-in strategy of MEV Elektronik due to their experience and know-how. Should further information about this topic be desired, please do not hesitate to contact one of the following persons:

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